ABSTRACT

A computer unit for a first (z) and a second (k, k*) number comprising at least one place shifting device (3, 4), whose shift position is controlled by an associated shift instruction (s1, s2) in dependence on the second number (k, k*), and to whose position inputs are conducted the value-ordered places of the first number (z), which generally is a binary coded dual number. The input or output of each place shifting device (s1, s2) has associated with it a sign inverter (5, 6), which is controlled by an associated sign instruction (n1, n2), in dependence on the second number (k, k*), which generally is a binary coded dual number using the canonical form, and on the output side, each place of the place shifting device (3, 4) is connected respectively to a place input of a four-place adder (7).